

Pipe Minus

By: Noah Wong

Based on "11.4 From SEQ+ to PIPE-"

Notes:

1. insnbits means "instruction word."
2. op means "opcode."
3. op stays in the writeback pipeline registers for status and control logging purposes.
4. format means the format of the instruction word, e.g. M, RR, RI, etc.
5. for PIPE-, data can only flow forward, so the values in red are passed to the next receiving CLB, not a previous one.
6. seq_succ means sequential successor, aka current_PC + 4.
7. correction_PC is current_PC + 4 if we mispredict a branch, since we predict branch_taken in B.cond.
8. M_opcode is included in the select_next_PC decision because if it's a B.cond, we need to look at the M_cond_val to decide what to do next.
9. D_opcode is included, because in the case of RET, we need to select the next PC, and val_a is included because that is where the return address gets calculated.

Select PC:

1. If M says mispredicted branch, use correction_PC
2. If D says RET, use val_a
3. Otherwise, use predicted_PC from F_instr

Pipeline registers:

1. adrp_val drops off as an option after decode because the result comes from just the current PC and the immediate, which are both available in Fetch. By the time the instruction moves into Decode, that value is already computed and just gets stored as the "seq_succ" field in D_instr.
2. seq_succ_PC drops off after execute because that's where generate_DMWX_control runs and where the next_PC prediction logic needs it. After that, it just becomes output of the ALU.
3. correction_PC survives all the way to Memory, because that's where cond_holds gets evaluated.

